

FIG. 2 is a cross-sectional view of a semiconductor device in accordance with the present invention. The device includes a substrate 40, a gate stack 42, a source/drain region 44, a channel region 46, a first conductive layer 48, a second conductive layer 50, a third conductive layer 52, a fourth conductive layer 54, a fifth conductive layer 56, a sixth conductive layer 58, a seventh conductive layer 60, an eighth conductive layer 62, a ninth conductive layer 64, a tenth conductive layer 66, and an eleventh conductive layer 68. The device is configured to provide a high-performance, low-power semiconductor device.

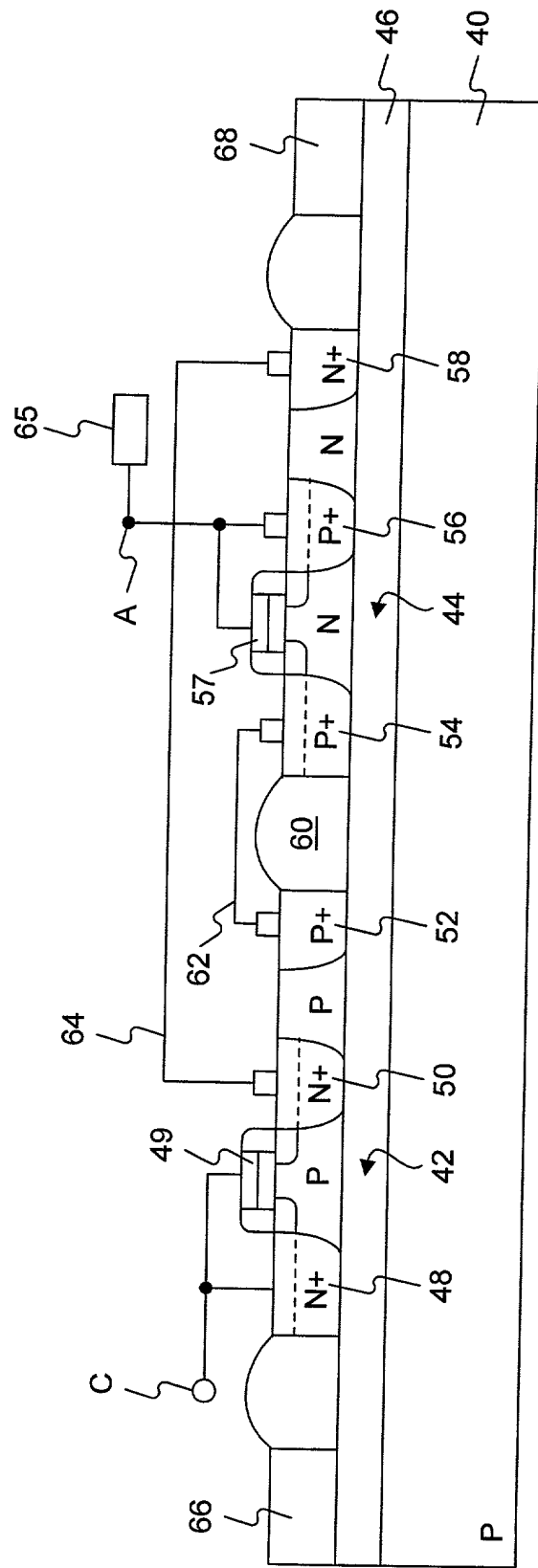


FIG. 2
(Prior Art)

FIG. 3 is a cross-sectional view of a semiconductor device in accordance with an embodiment of the present invention. The device includes a substrate 100, a first well 102, and a second well 104. The first well 102 is a P-well, and the second well 104 is an N-well. The device includes a first transistor 106 and a second transistor 108. The first transistor 106 is an NMOS transistor, and the second transistor 108 is a PMOS transistor. The first transistor 106 includes a gate 126, a source 110, a drain 112, and a channel 118. The second transistor 108 includes a gate 136, a source 130, a drain 132, and a channel 134. The device also includes a cathode 138 and an anode 140. The cathode 138 is connected to the source 110 of the first transistor 106, and the anode 140 is connected to the source 130 of the second transistor 108. The device further includes a first contact 122, a second contact 124, a third contact 128, and a fourth contact 144. The first contact 122 is connected to the gate 126 of the first transistor 106, the second contact 124 is connected to the gate 136 of the second transistor 108, the third contact 128 is connected to the drain 112 of the first transistor 106, and the fourth contact 144 is connected to the drain 132 of the second transistor 108. The device also includes a first isolation layer 110, a second isolation layer 112, a third isolation layer 114, and a fourth isolation layer 116. The first isolation layer 110 is located between the first transistor 106 and the second transistor 108, the second isolation layer 112 is located between the first transistor 106 and the first well 102, the third isolation layer 114 is located between the second transistor 108 and the second well 104, and the fourth isolation layer 116 is located between the second transistor 108 and the first well 102.

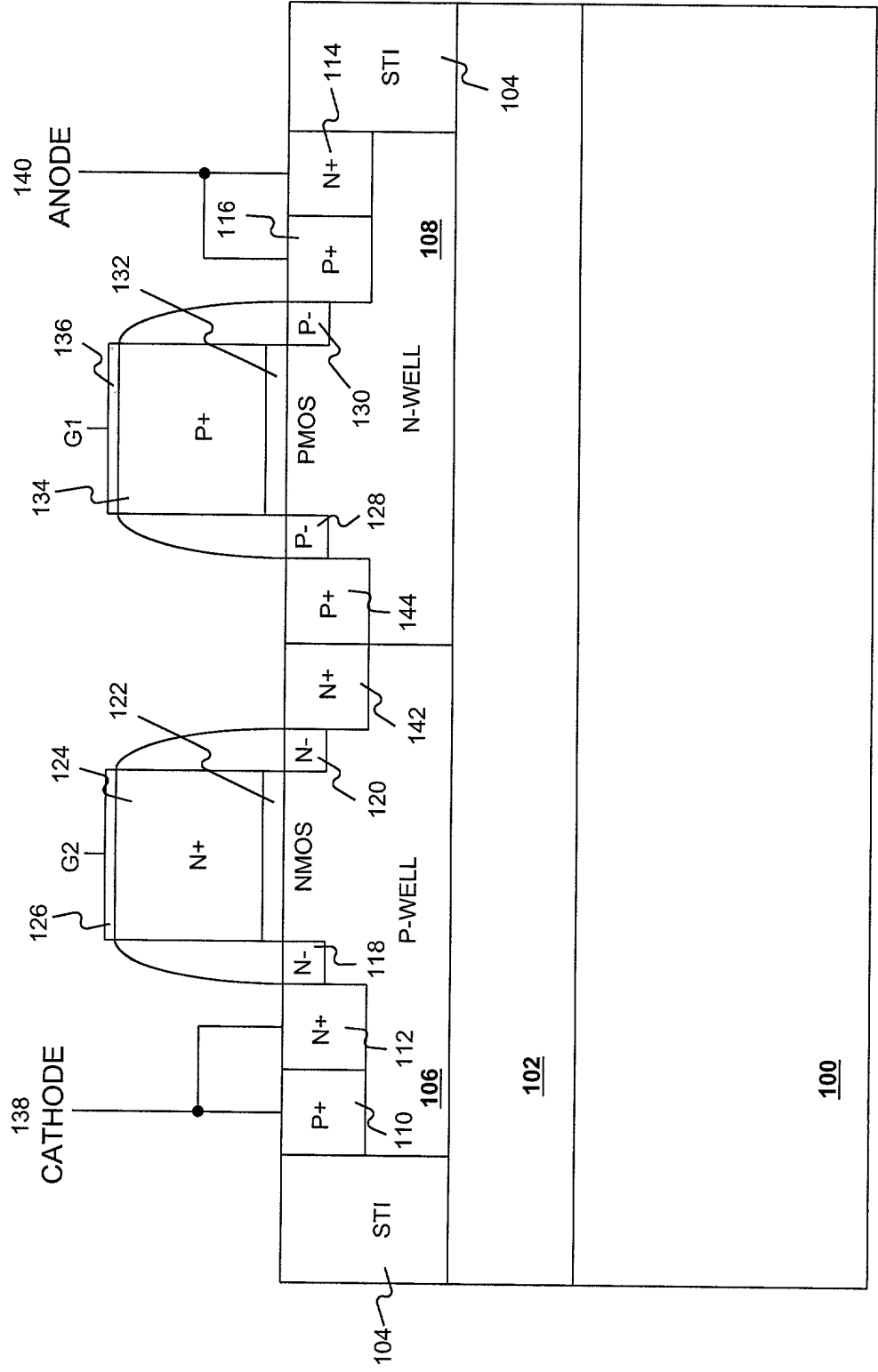


FIG. 3

US 2007/0172900 A1

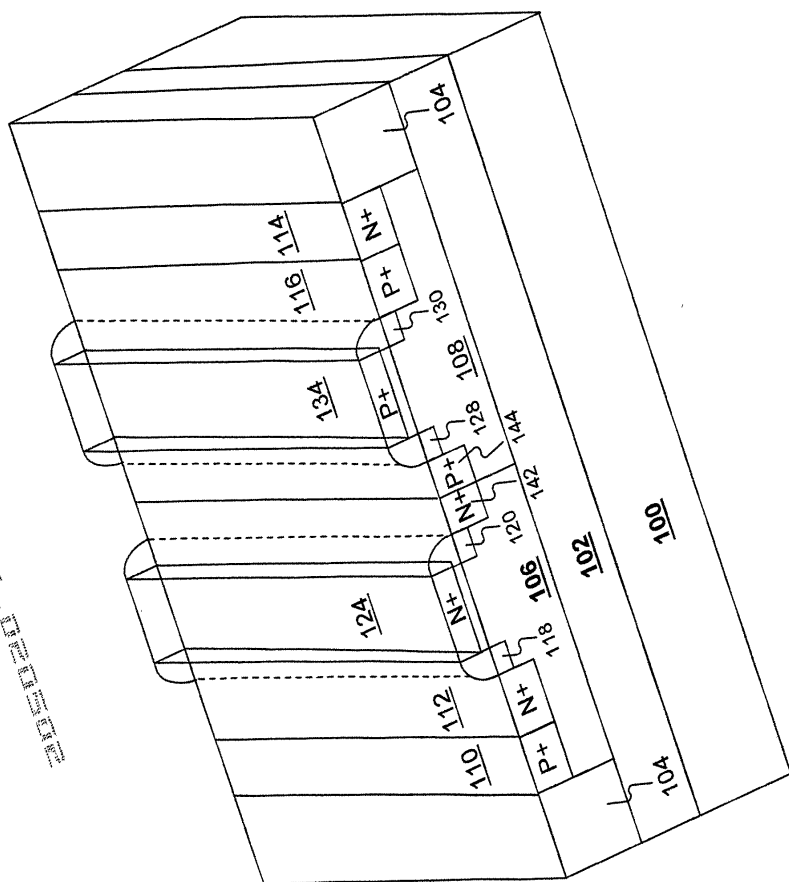


FIG. 4

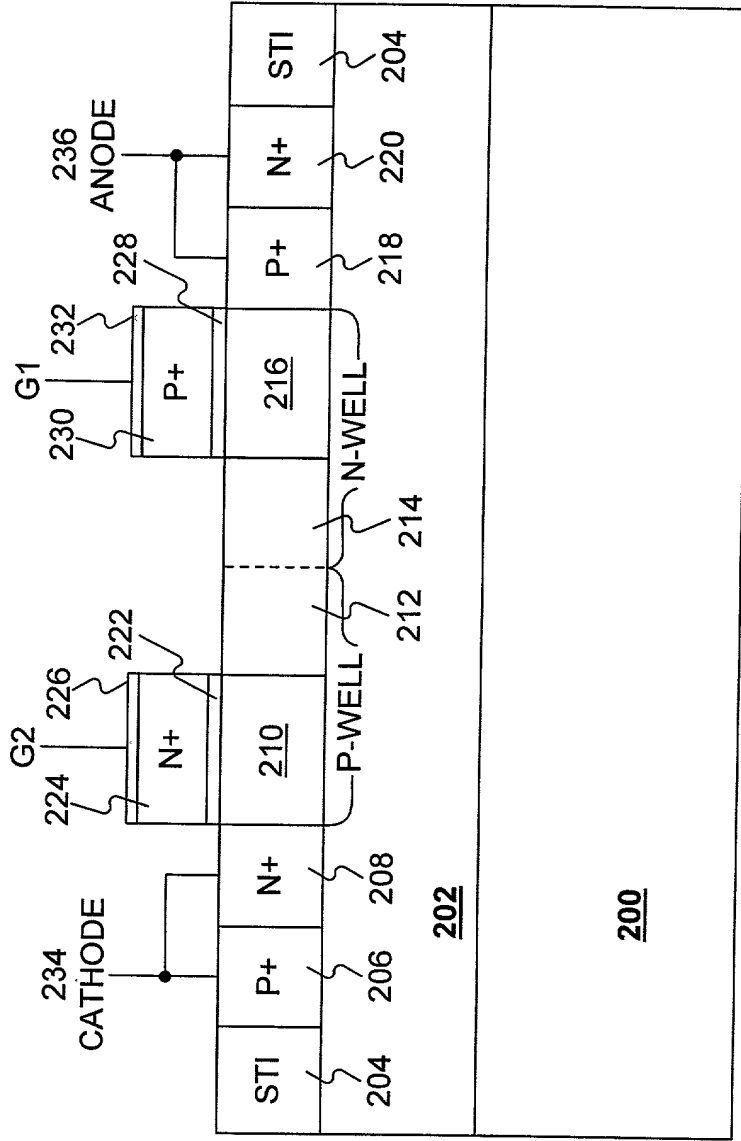


FIG. 5

FIG. 6 is a perspective view of a semiconductor device 200 in accordance with one embodiment of the present invention. The device 200 includes a substrate 202, a first layer 210, a second layer 216, and a third layer 220. The first layer 210 includes a first region 212 and a second region 214. The second layer 216 includes a first region 218 and a second region 220. The third layer 220 includes a first region 222 and a second region 224. The first region 212 is doped with N+ ions, the second region 214 is doped with P+ ions, the first region 218 is doped with N+ ions, the second region 220 is doped with P+ ions, the first region 222 is doped with N+ ions, and the second region 224 is doped with P+ ions. The device 200 also includes a first contact 204, a second contact 206, and a third contact 208. The first contact 204 is connected to the first region 212, the second contact 206 is connected to the second region 214, and the third contact 208 is connected to the first region 218. The device 200 is shown in a perspective view, with the substrate 202 at the bottom, the first layer 210 on top of the substrate, the second layer 216 on top of the first layer, and the third layer 220 on top of the second layer. The first contact 204 is located on the left side of the device, the second contact 206 is located on the right side, and the third contact 208 is located in the center. The first region 212 is located on the left side of the first layer, the second region 214 is located on the right side, the first region 218 is located on the left side of the second layer, and the second region 220 is located on the right side. The first region 222 is located on the left side of the third layer, and the second region 224 is located on the right side.

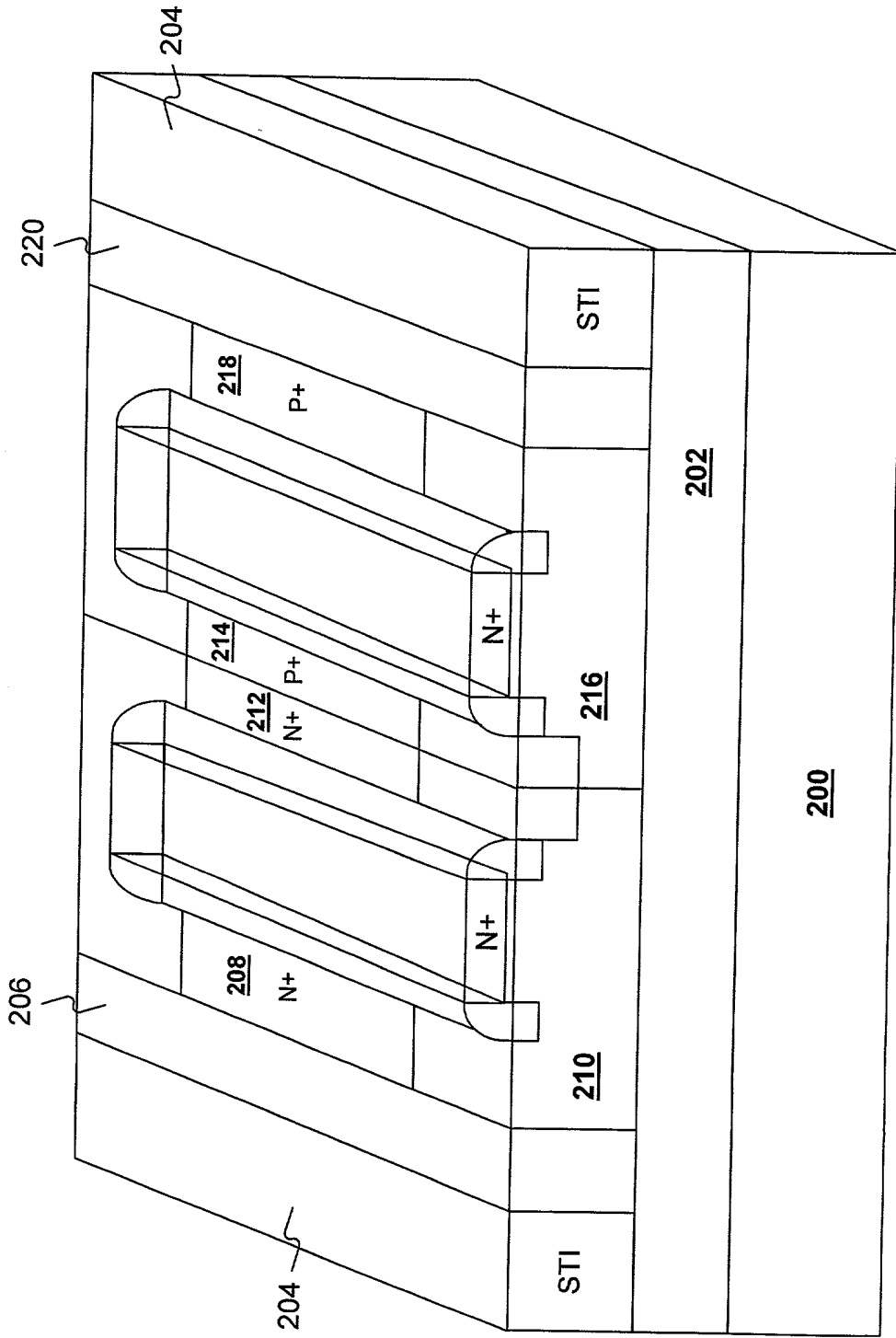


FIG. 6

FIG. 7A is a schematic diagram of a circuit for detecting an electrostatic discharge (ESD) event. The circuit includes a PAD (302) connected to an ESD DETECTING CIRCUIT (304) and an SOI-SCR (300). The ESD DETECTING CIRCUIT (304) is connected to the PAD (302) and the SOI-SCR (300). The SOI-SCR (300) is connected to the ESD DETECTING CIRCUIT (304) and has a gate (G1) connected to the ESD DETECTING CIRCUIT (304) and a gate (G2) connected to the PAD (302). The SOI-SCR (300) has a drain (140) connected to the PAD (302) and a source (138) connected to the ESD DETECTING CIRCUIT (304). The ESD DETECTING CIRCUIT (304) has an output (124) connected to the PAD (302) and an output (134) connected to the SOI-SCR (300).

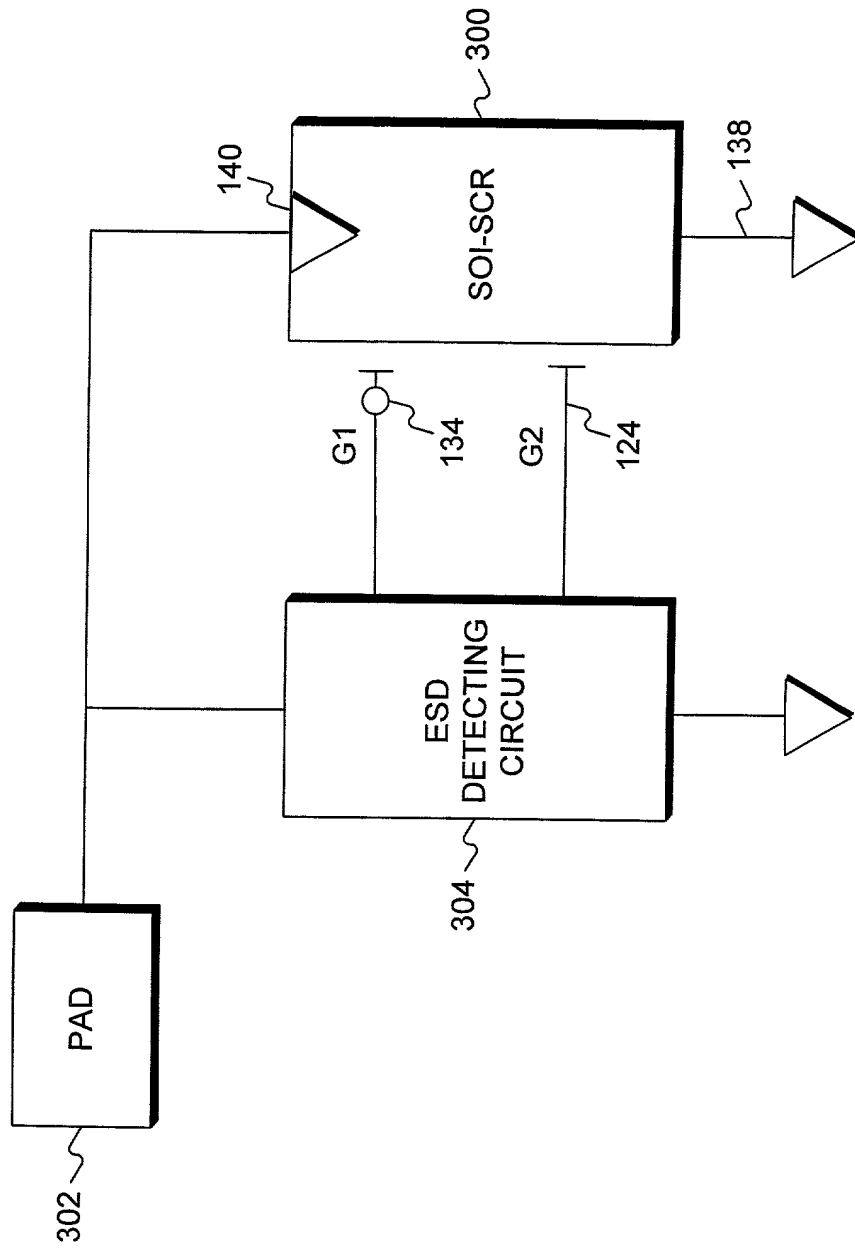


FIG. 7A

FIG. 7B is a schematic diagram of a circuit 300. The circuit 300 includes a PAD 302, a resistor 314, a capacitor 316, and a network of transistors and resistors. The circuit 300 is connected to a power supply 140 and a ground 138. The circuit 300 includes a first stage 304, a second stage 306, and a third stage 308. The first stage 304 includes a resistor 314, a capacitor 316, and a transistor 310. The second stage 306 includes a resistor 310-1, a resistor 310-2, a resistor 310-3, a resistor 312-1, a resistor 312-2, and a resistor 312-3. The third stage 308 includes a resistor 308-1, a resistor 308-2, and a resistor 308-3. The circuit 300 also includes a transistor 330, a transistor 332, and a transistor 334. The circuit 300 is connected to a power supply 140 and a ground 138. The circuit 300 includes a first stage 304, a second stage 306, and a third stage 308. The first stage 304 includes a resistor 314, a capacitor 316, and a transistor 310. The second stage 306 includes a resistor 310-1, a resistor 310-2, a resistor 310-3, a resistor 312-1, a resistor 312-2, and a resistor 312-3. The third stage 308 includes a resistor 308-1, a resistor 308-2, and a resistor 308-3. The circuit 300 also includes a transistor 330, a transistor 332, and a transistor 334. The circuit 300 is connected to a power supply 140 and a ground 138.

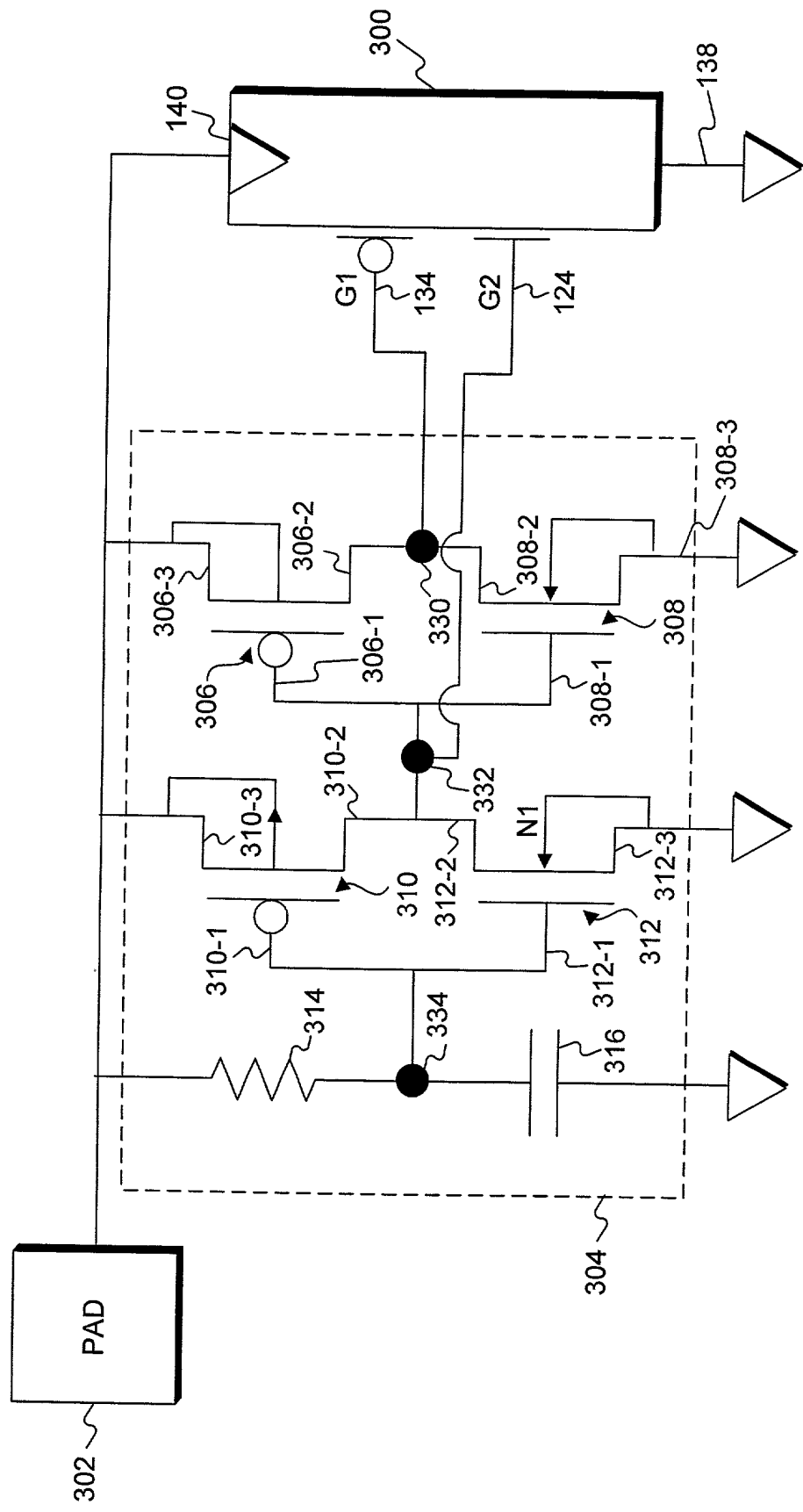


FIG. 7B

FIG. 8A is a schematic diagram of a circuit 300. The circuit 300 includes a first block 304' and a second block 300. The first block 304' is connected to a VDD supply and a VSS supply. The second block 300 is connected to the VDD supply and the VSS supply. The circuit 300 also includes a first gate G1 and a second gate G2. The first gate G1 is connected to the VDD supply and the first block 304'. The second gate G2 is connected to the VDD supply and the second block 300. The circuit 300 further includes a first diode D1, a second diode D2, and a third diode DN. The first diode D1 is connected to the VDD supply and the first block 304'. The second diode D2 is connected to the VDD supply and the second block 300. The third diode DN is connected to the VDD supply and the VSS supply.

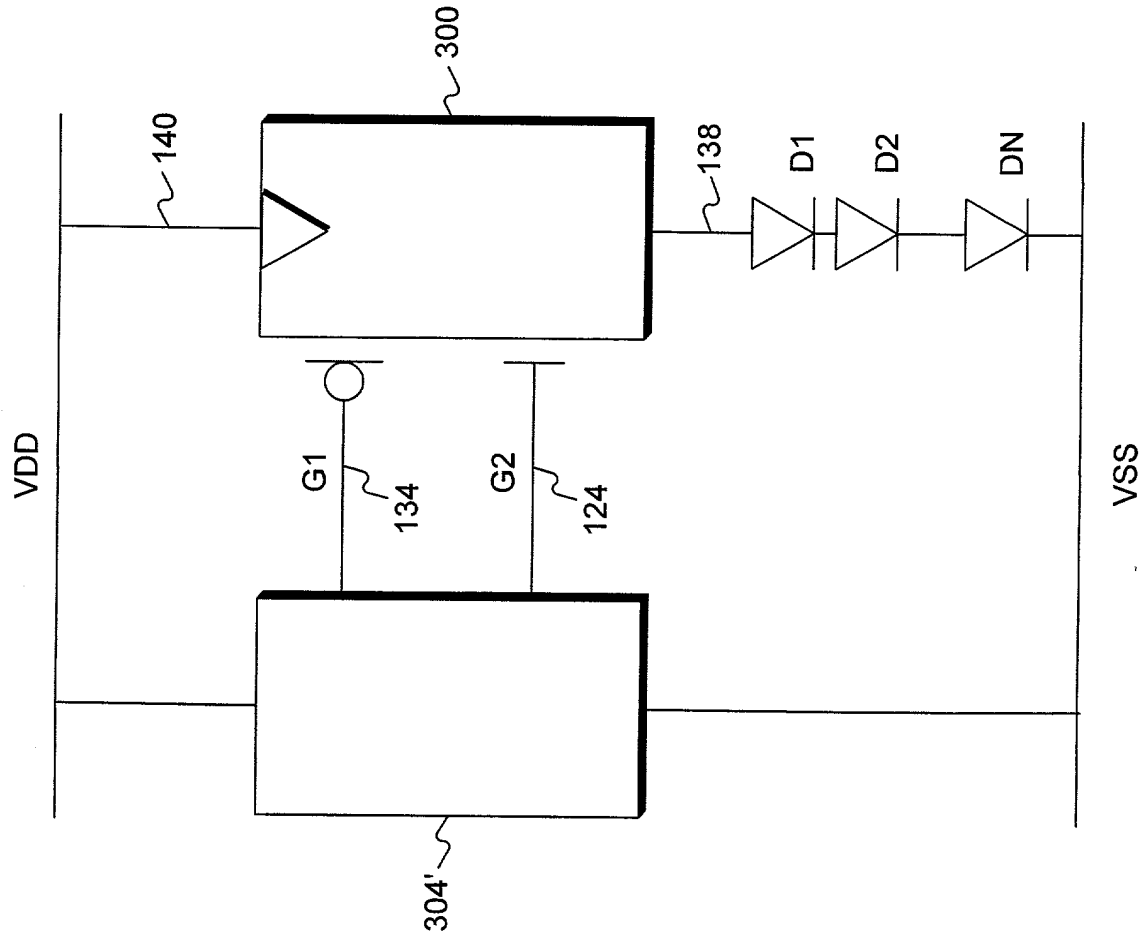


FIG. 8A

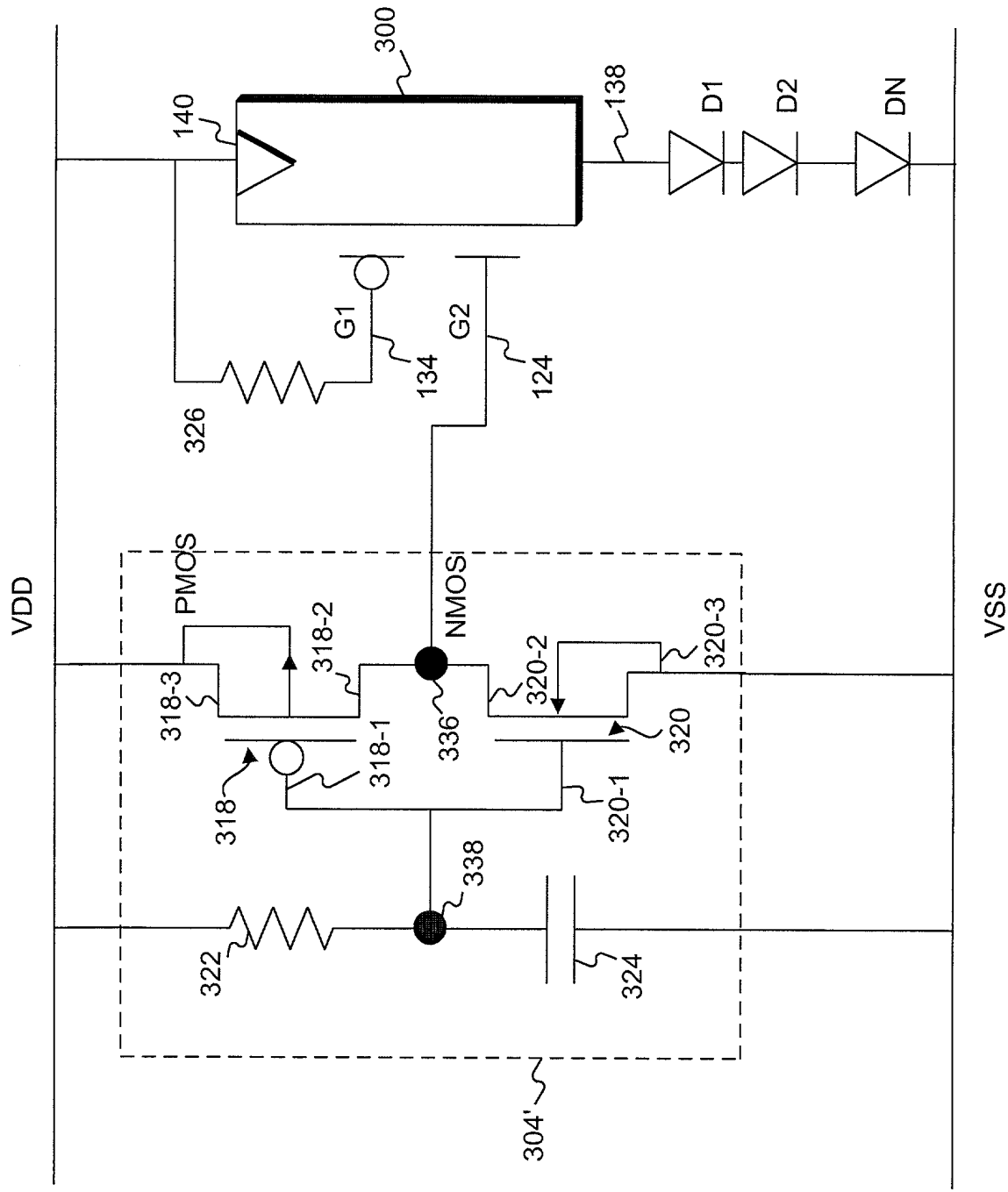


FIG. 8B